IEEE Catalog Number : CFP1469E-USB ISBN : 978-1-4799-5126-0

Time Table

Monday ~ Tuesday, November 3~4, 2014

Nov. 3 Monday			Time		Nov. 4 Tuesday							
Lobby	Ballroom 2	Ballroom 3	From	Till	Ballroom 1	Ballroom 2	Ballroom 3	Ballroom 4	Mara	Udo	Chuja	Lobby
			9:00	9:15		ETRI Aldebaran Demo	CDC-1	CDC-2	CDC-3	CDC-4	CDC-5	CDC & ETRI Demo & Panel 1
			9:15	9:30								
			9:30	9:45								
			9:45	10:00	Break							
			10:00	10:15	Opening Ceremony							
			10:15	11:00	Keynote - 1							
			11:00	11:45	Keynote - 2							
			11:45	12:30	Keynote - 3							
			12:30	13:30	Lunch							
			13:30	13:35		ETRI Aldebaran Demo	A1	346	DV	574	ET	585	LP	218	SS-A	721	CDC & ETRI Demo & Panel 2
			13:35	13:50				572		1191		189		1068		1155	
			13:50	14:05				369		364		655		486		1165	
			14:05	14:20				123		1003		145		192		1169	
			14:20	14:35				841		1052		391		967		1159	
			14:35	14:50						1060		742		225			
			14:50	15:05	CDC Tour Break												
			15:05	15:20													
			15:20	15:35													
Registration	Tutorial 1-1	Tutorial 2-1	15:35	15:50		ETRI Aldebaran Demo	COSAR Workshop		SS-B		SS-C	748		788	SS-D	1147	
			15:50	16:05								755		558		1143	
			16:05	16:20								569		1138		1086	
	Break		16:20	16:35								753		793		630	
			16:35	16:50								743		658		611	
	Tutorial 1-2	Tutorial 2-2	16:50	17:05								640					
			17:05	17:20								1021					
			17:20	18:00	Break												
			18:00	18:20	Banquet												
			18:20	18:30													
			18:30	19:00													
Welcome Reception			19:00	20:00													

A1 Analog and Mixed-Signal Techniques I
DV Digital Circuits and VLSI Architectures
ET Emerging technology
LP Power Electronics / Energy Harvesting Circuits
SS-A Invited Special Session: Near-Threshold Voltage Circuit Design
SS-B Invited Special Session: Image Signal Processing for Vision/Multimedia SoC
SS-C Invited Special Session: Analog/Digital Circuits for Mobile SoC
SS-D Invited Special Session: Design, Analysis and Tools for Integrated Circuits and Systems (DATICS)

Jin-Gyu Kang, and Changsik Yoo
Hanyang University, Korea

[CDC5-3] 12.5-Gb/s Monolithic Optical Receiver with CMOS Avalanche Photodetector
Hyun-Yong Jung, Jeong-Min Lee, Jin-Sung Youn, and Woo-Young Choi
Yonsei University, Korea

CDC Panel Session 1

09:00~13:00 Lobby
Chair: Kyoung Rok Cho *(Chungbuk National University, Korea)*
Kwang Hyun Baek *(Chung-Ang University, Korea)*

CDC(P)-1 Load Independent Charge Control of Single-Inductor Multiple-Output DC-DC Converter
Young-Jin Moon, Jeongpyo Park, Min-Gyu Jeong, Sang-Hyun Kim, Jin-Gyu Kang, and Changsik Yoo
Hanyang University, Korea

CDC(P)-2 Active Power Factor Correction (PFC) Circuit with Resistor-Free Zero Current Detection
Yong-Seong Roh, Young-Jin Moon, Jeongpyo Park, Min-Gyu Jeong, Sang-Hyun Kim, Jin-Gyu Kang, and Changsik Yoo
Hanyang University, Korea

CDC(P)-3 A 100-kS/s 8.3-ENOB 1.7-uW Time-Domain Analog-to-Digital Converter
Younghoon Kim and Changsik Yoo
Hanyang University, Korea

CDC(P)-4 A Zero-Skew All-Digital Fractional-Ratio Multiplying Delay-Locked Loop
Sangwoo Han and Jongsun Kim
Hongik University, Korea

CDC(P)-5 "A 6.78 Mhz 5W Wireless Power Transfer Active Rectifier for Mobile Charger"
Kye-Seok Yoon and Gyu-Hyeong Cho
Korea Advanced Institute of Science and Technology(KAIST), Korea

CDC(P)-6 A Compact On-chip Passive Equalizer for High-speed Differential Data Transmission
Heegon Kim, Sumin Choi, Jonghoon J. Kim, Sukjin Kim, and Joungho Kim
Korea Advanced Institute of Science and Technology(KAIST), Korea

CDC(P)-7 Hybrid-domain Two-step Time-to-Digital Converter Using Switch-Based Time-to-Voltage converter and SAR-ADC
Jung-ho Kim and SeongHwan Cho
Korea Advanced Institute of Science and Technology(KAIST), Korea

CDC(P)-8 A Fully Integrated Phase-Locked Loop with Leakage Current Compensation in 65-nm CMOS Technology
Jinhoon Hyun and Soo-Won Kim
Korea University, Korea

CDC(P)-9 Power and Area Efficient Li-ion Battery Charger IC

12.5-Gb/s Monolithic Optical Receiver with CMOS Avalanche Photodetector

Hyun-Yong Jung, Jeong-Min Lee, Jin-Sung Youn, and Woo-Young Choi
Department of Electrical and Electronic Engineering, Yonsei University, Seoul 120-749, South Korea
hyjunghyjung@gmail.com

I. Introduction

Recently, optical interconnect technology is receiving a great amount of research attention as it can overcome the limitation of electrical interconnects. High-speed monolithic optical receivers have been reported with various types of photodetectors and on-chip electrical equalizers [1, 2]. We present a CMOS optical receiver having a 850-nm CMOS avalanche photodetector along with underdamped transimpedance amplifier (TIA) that can operate up to 12.5-Gb/s operation.

II. Description.

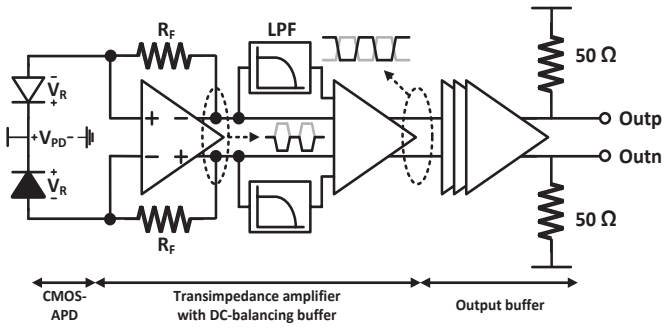


Fig. 1. Block diagram of the optical receiver.

Fig. 1 shows a block diagram of our optical receiver. Fig. 1(a) shows a simplified block diagram of our optical receiver. It is composed of a CMOS-avalanche photodetector (APD) with a dummy PD, a shunt-feedback TIA with DC-balancing buffer, and an output buffer with 50-Ω load. The dummy PD provides symmetric capacitive load to the differential TIA input. The photo-detection bandwidth of our CMOS-APD is limited by the transit time of slow diffusive photocurrents. This leads to the bandwidth limit of the optical receiver even with a high-speed TIA. To compensate this, we use an underdamped TIA which can be realized by decreasing the core-amplifier bandwidth of shunt-feedback TIA. Photo-generated currents generate TIA differential output with a DC offset which can cause decision threshold problem. To eliminate this problem, a DC-balancing buffer is added.

III. Chip Implementaion and Results

Fig. 2 shows the micro photograph of the fabricated optical receiver in 65-nm CMOS technology. The core size is 0.24 × 0.1 mm^2, and the power consumption of the electronic circuit excluding output buffer is about 13.7 mW with 1.2-V supply

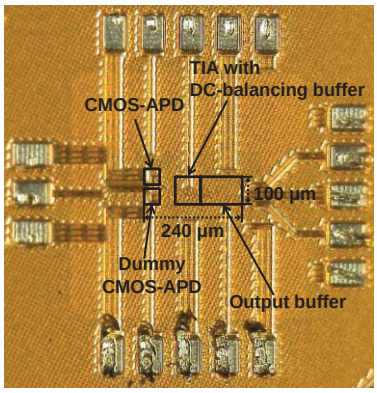


Fig. 2. Microphotograph of the fabricated optical receiver.

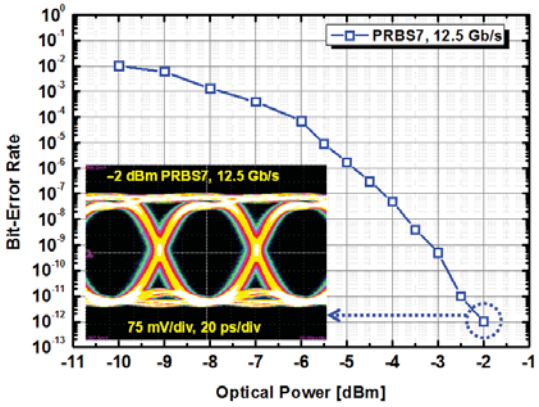


Fig. 3. Measured BER performance and eye diagram of transmitted 12.5-Gb/s data.

voltage. With the optical receiver, 12.5-Gb/s optical data are successfully detected. Fig. 4 shows the measured BER performance and the inset in Fig. 4 shows the measured eye diagram for 12.5-Gb/s optical data with −2-dBm incident optical power.

Reference

[1] S.-H. Huang, W.-Z. Chen, Y.-W. Chang, and Y.-T Huang, "A 10-Gb/s OEIC with meshed spatially-mudulated photo detector in 0.18-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1158-1169, May 2011.

[2] J.-S. Youn, M.-J. Lee, K.-Y. Park, and W.-Y. Choi, "10-Gb/s 850-nm CMOS OEIC receiver with a silicon avalanche photodetector," *IEEE J. Quantum Electron.*, vol. 48, no. 2, pp. 229-236, Feb. 2012.

This work [2012R1A2A1A01009233] was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MEST). The authors are very thankful to IC Design Education Center (IDEC) for EDA software support as well as chip fabrication.

ISOCC 2014 Chip Design Contest

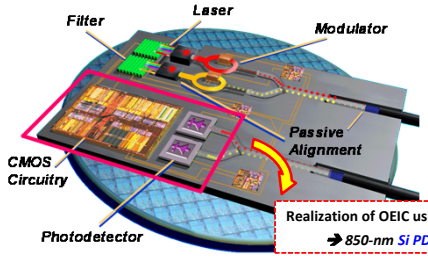
12.5-Gb/s Monolithically Integrated Optical Receiver with CMOS Avalanche Photodetector

H.-Y. Jung,[1] J.-M. Lee,[1] J.-S. Youn,[1] W.-Y. Choi,[1] and M.-J. Lee [2]

[1]Department of Electrical and Electronic Engineering, Yonsei University, Seoul, Korea

[2]Faculty of Electrical Engineering, Delft University of Technology, Delft, Netherlands

Introduction & Previous Works



(Ref. Intel, 2006)

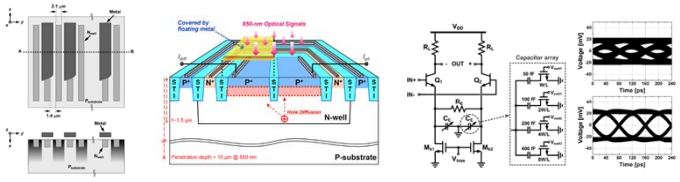
Realization of OEIC using standard Si technology
➔ *850-nm Si PD + Electronic Circuits*

- Copper-based electrical interconnect ➔ Interconnect bottleneck !
- Optical interconnect
  - Realization in a cost-effective manner
  - Integration with existing systems
  - Compatibility with Si technology

  ➔ Silicon Photonics !

- Compensation of bandwidth limitation of Si PDs

10 Gb/s JSTQE 2011 *12.5 Gb/s OE 2014* *12.5 Gb/s OE 2012*

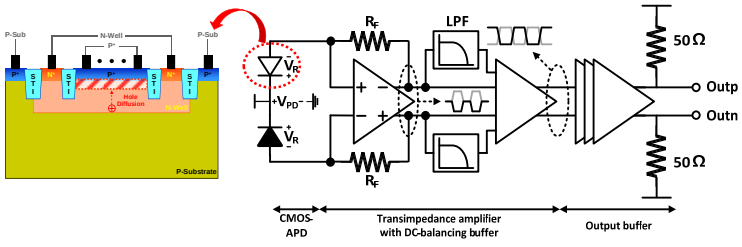


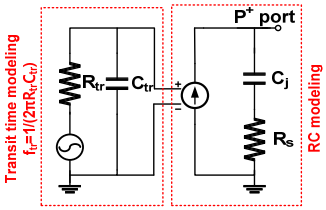
<Spatially-modulated photodetector > <Equalizer>

- SM PD: Decreasing diffusion current ➔Speed ↑
  Low responsivity
- Equalizer: Electrical enhancement of bandwidth
  Additional power and area

➔ Bandwidth enhancement by *Underdamped TIA*

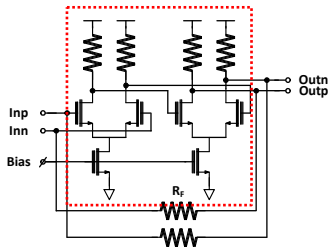
CMOS Optical Receiver



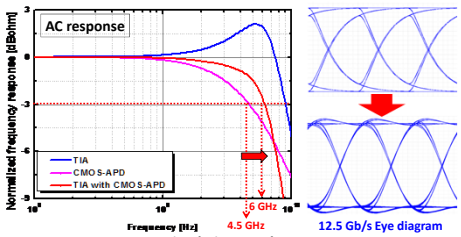


<CMOS-APD modeling>

Core amplifier



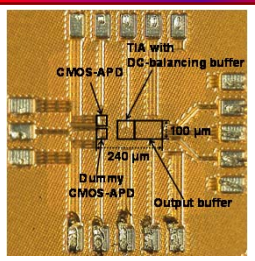
<TIA Schematic>



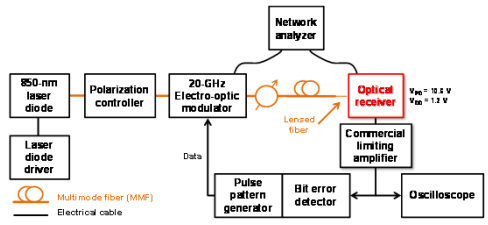
<Simultaion Results>

- Standard 65-nm CMOS technology (Samsung)
- On-chip CMOS-compatible avalanche photodetector (APD)
  - P+/N-well junction PD without slow diffusion currents
  - Active area (10 μm x 10 μm): RC time constant reduction
- Under-damped transimpedance amplifier (TIA) for BW enhancement
- DC-balancing buffer: f_T doubler structure

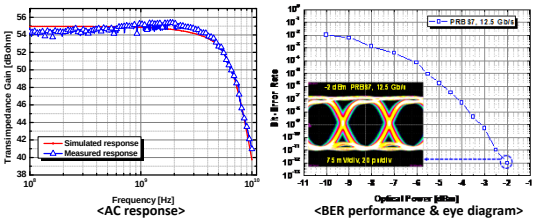
Measurement Results



<Chip photograph>



<Measurement setup>



<AC response> <BER performance & eye diagram>

	10' JSSC	11' JSSC	12' JQE	14' OE	This work
Technology	130-nm CMOS	180-nm CMOS	130-nm CMOS	130-nm CMOS	65-nm CMOS
Structure	SM-PD + TIA + EQ +LA	SM-PD + TIA + LA (9 passive inductors)	APD + TIA + EQ + LA	SM-APD + TIA + EQ + LA	APD + TIA
Data rate	8.5 Gb/s	10 Gb/s	10 Gb/s	12.5 Gb/s	12.5 Gb/s
Sensitivity	-3.2 dBm (10^{-12})	-6 dBm (10^{-11})	-4 dBm (10^{-12})	0 dBm (10^{-12})	-2 dBm (10^{-12})
Supply voltage	1.5 V	1.8 V (Circuit) 14.2 V (PD)	1.2 V (Circuit) 10.5 V (PD)	1.3 V (Circuit) 10.5 V (PD)	1.2 V (Circuit) 10.6 V (PD)
Power (Excluding output buffer)	47 mW	118 mW	66.8 mW	72.4 mW	13.7 mW (without LA)
Chip area	0.1 mm^2	0.76 mm^2	0.26 mm^2	0.26 mm^2	0.024 mm^2

Conclusion

- 850-nm CMOS fully integrated optical receiver demonstration
- Bandwidth enhancement by under-damped TIA
- Successful 12.5-Gb/s operation with BER of 10^{-12} at -2 dBm incident optical power